This listing of claims will replace all prior versions, and listing, of claims in th application:

Listing of claims:

1. (Cancelled)

2. (Currently Amended) An integrated circuit design kit comprising:
means for generating one or more circuit component topologies; and
means for designing one or more ~~critical interconnect~~ transmission line topologies.

3. (Currently Amended) The kit of claim 2 wherein said ~~interconnect~~ transmission line topologies are predefined.

4. (Previously Presented) The kit of claim 2 and further comprising one or more circuit component models.

5. (Currently Amended) The kit of claim 2 and further comprising one or more ~~critical interconnect~~ transmission line models.

6. (Currently Amended) A design topology of ~~critical interconnect~~ transmission lines.

7. (Previously Presented) The design topology of claim 6 wherein said topology is predefined.

8. (Previously Presented) The design topology of claim 6 comprising a definite current return path.

9. (Previously Presented) The design topology of claim 6 wherein said design topology comprises a model describing one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters.

10. (Cancelled)

11. (Previously Presented) The design topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires.

12. (Previously Presented) The design topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires.

13. (Previously Presented) The design topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire.

14. (Previously Presented) The design topology of claim 11 and wherein said one or more shielding wires is one or more shielding layers.

15. (Currently Amended) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of ~~critical interconnect~~ transmission lines.

16. (Currently Amended) The product of claim 15 and further comprising instructions, which when read by a computer, cause said computer to create a design model of ~~critical interconnect~~ transmission lines.

17. (Currently Amended) A computer software circuit design product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which when read by a computer, cause said computer to deploy said circuit design product, said circuit design product comprising means for designing topology of ~~critical interconnect~~ transmission lines.

18. (Currently Amended) The product of claim 17 and further comprising instructions, which when read by a computer, cause said computer to create a design mod l of ~~critical interconnect~~ transmission lines.

19. (Cancelled)

20. (Cancelled).

21. (Cancelled)

22. (Previously Presented) The method of claim 32, wherein said integrated circuits are analog and mixed signal (AMS) circuits or application specific integrated circuits (ASIC).

23. (Previously Presented) The method of claim 32, wherein in (b), the step of defining comprises choosing from a set of predefined parameterized design topologies.

24. (Previously Presented) The method of claim 32, wherein in (b), the step of defining comprises defining a set of design topologies.

25. (Previously Presented) The method according to claim 32, wherein said schematic design comprises models of said one or more transmission line topologies.

26. (Original) The method according to claim 25, and further comprising the step of calculating one or more electrical parameters of said models.

27. (Original) The method according to claim 26, wherein said one or more electrical parameters includes one or more of the following: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters.

28. (Previously Presented) The method according to claim 32, wherein step (b) comprises:

using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, signal integrity, timing requirements and manual user selection.

29. (Previously Presented) The method according to claim 25, and further comprising creating parameterized cells from said models.

30. (Original) A method for designing integrated circuits wherein defining said chip architecture and a floor plan comprises defining critical interconnect wires.

31. (Currently Amended) A system for integrated circuit design comprising:

means for designing a high level circuit design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks and their locations are defined, and further including one or more ~~critical interconnect~~ transmission line ~~wire~~ topologies;

means for designing a schematic design at least including one or more circuit components and one or more ~~critical interconnect~~ transmission line ~~wire~~ models; and

means for designing a physical layout at least said one or more circuit components and said one or more ~~critical interconnect~~ transmission line topologies.

32. (Currently Amended) A method for designing integrated circuits (IC), said method comprising the steps of:

(a) defining a chip architecture and a floor plan;

(b) identifying one or more critical interconnect lines, and defining one or more transmission line topologies for design of said critical interconnect lines;

(c) determining a schematic design of said IC from said chip architecture floor plan and said ~~critical interconnect~~ transmission line topologies; and

(d) defining a physical layout of said IC at least from said chip architecture floor plan and said ~~critical interconnect~~ transmission line topologies.

33. (Currently Amended) The method according to claim 32, wherein said physical design comprises parameterized cells of said one or more transmission line topologies.

34. (Currently Amended) A system for integrated circuit design comprising:

means for designing a schematic design at least including one or mor circuit components and one or more ~~critical interconnect~~ transmission wire models, wherein said one or more ~~critical interconnect~~ transmission wire models are parameterized cells of one or more transmission line topologies.

35. (Currently Amended) A system for integrated circuit design comprising:

means for designing a schematic design; and

means for designing a physical layout including at least one or more circuit components and one or more ~~critical interconnect~~ transmission line ~~wire~~ topologies, wherein said one or more ~~critical interconnect wire~~ transmission line topologies are parameterized cells of transmission lines.